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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,121	ALBEROLA ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-9,11,12,14-17 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-9,11,12,14-17 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/26/2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 5-9, 11-12, 14-17, 21-24 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 1/24/2007.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations for claims 1, 8, 16, and 21 reciting "determining, based on said executing, that a second instruction subsequent to the first instruction will not be executed" and "arranging for a pre-decoded second instruction to not be provided from the direct memory access unit to the processing element" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Claim objections

4. Claim 21 is objected to because of the following informalities:

5. Claim 21 recites "without sending the pre-decoded second via ..." and should be replaced with "without sending the pre-decoded second instruction via ..."

New Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 5-9, 11, and 14-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041).

8. As per claim 1:

Kotani disclosed a method, comprising:

Retrieving a first instruction from a memory unit via an n-bit input path (Kotani: Figure 9 element 20, column 10 lines 25-48)(The DMA unit receives drawing data and commands from main memory to transfer to the processing unit. It's inherent that the instructions received by DMA unit are received via a n-bit bus.);

Pre-decoding the first instruction at a direct memory access unit (Kotani: Figure 9 element 234, column 11 lines 51-64)(The DMA pre-decodes instructions in order to look for interrupts before transferring the instructions and data to the processing unit.); and

Providing the pre-decoded first instruction from the direct memory access unit to a processing element via a q-bit output path (Kotani: Figure 9 element 232, column 10 lines 34-48 and column 11 lines 51-64)(The DMA pre-decodes instructions in order to look for interrupts before transferring the instructions and data to the processing unit, either directly or through the local memory element 40 in figure 9. It's inherent that the instructions received by DMA unit are sent out via a q-bit bus).

Decoding the pre-decoded first instruction at the processing element (Kotani: Figure 9 element 232, column 10 lines 34-48)(It's inherent that the processing element fully decodes the command instruction in order to know how the instructions are supposed to operate in the drawing unit.); and

Executing the decoded instruction via a processor pipeline (Kotani: Figure 9 element 232, column 10 lines 34-48)(The drawing unit inherently executes the instructions it receives.).

Determining, based on said executing, that a second instruction subsequent to the first instruction will not be executed (Kotani: Figure 11 element 239, column 11 lines 20-28)(The drawing end instruction tells that there are no further instructions to execute in the current path. It's obvious to one of ordinary skill in the art that the DMA controller will continually fetch instructions from a current memory area until told to do otherwise. Therefore, the DMA will only be told to do so otherwise at the very earliest when the drawing end instruction is predecoded within the DMA. Since Kotani doesn't disclose the predecoder being used for detecting the drawing end instruction, it's obvious to one of ordinary skill in the art that the drawing end instruction may not be detected until it's fully decoded in the processor. Thus, it would have been obvious to one of ordinary skill in the art that at least one more instruction would have been fetched from memory during the predecoding process, which leaves at least one instruction within the DMA that won't be executed because the drawing has finished processing.); and

Arranging for a pre-decoded second instruction to not be provided from the direct memory access unit to the processing element (Kotani: Figure 11 element 239, column

11 lines 20-28)(The drawing end instruction tells that there are no further instructions to execute in the current path. It's obvious to one of ordinary skill in the art that the DMA controller will continually fetch instructions from a current memory area until told to do otherwise. Therefore, the DMA will only be told to do so otherwise at the very earliest when the drawing end instruction is predecoded within the DMA. Since Kotani doesn't disclose the predecoder being used for detecting the drawing end instruction, it's obvious to one of ordinary skill in the art that the drawing end instruction may not be detected until it's fully decoded in the processor. Thus, it would have been obvious to one of ordinary skill in the art that at least one more instruction would have been fetched from memory during the predecoding process, which leaves at least one instruction within the DMA that won't be executed because the drawing has finished processing. Also, it's obvious to one of ordinary skill in the art that this instruction would come into the DMA and be predecoded in the next cycle.).

Kotani failed to teach where the n-bit input path is less than the q-bit output path;.

However, Pechanek disclosed where the n-bit input path is less than the q-bit output path (Pechanek: Figure 5 element 512, column 10 lines 37-43)(An example instruction, the add instruction, is predecoded by element 512, which generates control signals. When in combination with Kotani, these control signals would also be sent with the instruction to the processor, which results in a larger output path than the input path.).

Kotani is silent on the details of how predecoding works. Pechanek describes the details of predecoding an instruction that results in control signals for the processor

being generated by the predecoder. One of ordinary skill in the art would have been motivated to find out how predecoding works to find the processor of Pechanek that describes in detail the generation of control signals for instructions to add this functionality. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add the control signal generation aspect of Pechanek for the advantage of realizing how predecoding works.

9. As per claim 2:

Kotani and Pechanek disclosed the method of claim 1, wherein said providing comprises storing the pre-decoded first instruction in memory local to the processing element (Kotani: Figure 9 element 40, column 10 lines 34-48 and column 11 lines 51-64)(The DMA pre-decodes instructions in order to look for interrupts before transferring the instructions and data to the processing unit, either directly or through the local memory element 40 in figure 9.).

10. As per claim 5:

Kotani and Pechanek disclosed the method of claim 1, further comprising:

Loading instructions into the memory unit during a boot-up process (Official notice is taken that instructions are loaded into a memory unit during a boot-up process.).

11. As per claim 6:

Kotani and Pechanek disclosed the method of claim 1, wherein the processing element is a reduced instruction set computer device (Official notice is taken that the processing element could be modified to run a RISC processor architecture.).

12. As per claim 7:

Kotani and Pechanek disclosed the method of claim 6, wherein the pre-decoded instruction comprises execution control signals (Kotani: Figure 11 element 241-242, column 11 lines 29-40)(The DMA unit pre-decodes interrupts and sends control signals back to the host processor.).

13. As per claim 8:

Claim 8 essentially recites the same limitations of claim 1. Therefore, claim 8 is rejected for the same reasons as claim 1.

14. As per claim 9:

Claim 9 essentially recites the same limitations of claim 8. Therefore, claim 9 is rejected for the same reasons as claim 8.

15. As per claim 11:

The additional limitations of claim 11 essentially recite the additional limitations of claim 2. Therefore, claim 11 is rejected for the same reasons as claim 2.

16. As per claim 14:

Kotani and Pechanek disclosed the apparatus of claim 8, wherein the direct memory access unit, the memory unit, and the processing element are formed on an integrated circuit (Official notice is taken that the DMA, memory, and PE's are formed on an integrated circuit.).

17. As per claim 15:

The additional limitations of claim 15 essentially recite the additional limitations of claim 6. Therefore, claim 15 is rejected for the same reasons as claim 6.

18. As per claim 16:

Claim 16 essentially recites the same limitations of claim 1. Therefore, claim 16 is rejected for the same reasons as claim 1.

19. As per claim 17:

Claim 17 essentially recites the same limitations of claim 2. Therefore, claim 17 is rejected for the same reasons as claim 2.

20. Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041), further in view of Kessler et al. (U.S. 6,738,836).

21. As per claim 12:

Kotani and Pechanek disclosed the apparatus of claim 10, including a plurality of processing elements, each processing element being associated with a direct memory access unit that includes an instruction pre-decoder (Kotani: Figure 9 elements 232 and 234, column 10 lines 34-48 and column 11 lines 51-64).

Kotani and Pechanek failed to teach a plurality of processing elements.

However, Kessler disclosed including a plurality of processing elements (Kessler: Figure 1 element 100, column 4 lines 32-50)(Figure 1 shows a plurality of processing elements that the single processing element of Kotani could be arranged in.).

The advantage of using a large number of processing elements in parallel is that they are able to solve complex computational problems in a reasonable amount of time (Kessler: Column 2 lines 6-14). One of ordinary skill in the art at the time of the

invention would have been motivated to implement a parallel computing machine comprised of processing elements of Kotani for the benefits of increased performance. Thus, one of ordinary skill in the art at the time of the invention would have made the processing element of Kotani into many elements of a large parallel computing structure for the advantage of increased performance.

22. Claim 21 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041), further in view of Ramsdale et al. (U.S. 5,265,263).

23. As per claim 21:

Claim 21 essentially recites the same limitations of claim 1. Claim 21 additionally recites the following limitations:

Kotani and Pechanek failed to teach a multi-directional antenna.

However, Ramsdale disclosed a multi-directional antenna (Ramsdale: Figures 1a and 1b, element 1, column 2 lines 4-13).

The advantage of having a multi-directional antenna is that it allows wireless communication between devices. One of ordinary skill in the art would have been motivated to add a multi-directional antenna to allow for wireless communication between devices. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a multi-directional antenna to allow for the processor of Kotani to have the ability to communicate wirelessly.

24. Claims 22-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041), in view of Ramsdale et al. (U.S. 5,265,263), further in view of Funderbunk et al. (U.S. 5,291,525)

25. As per claim 22:

Kotani, Pechanek, and Ramsdale disclosed the system of claim 21.

Kotani, Pechanek, and Ramsdale failed to teach wherein the apparatus is a digital base band processor.

However, Funderbunk disclosed wherein the apparatus is a digital base band processor (Funderbunk: Figure 1, column 3 lines 50-67 continued to column 4 lines 1-37).

Base band is a method of signal transmission. The advantage of using base band is that it has a simple implementation because the signals are transmitted without frequency divisions. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the processor as a digital base band processor for the advantage of a simple implementation of transmitting signals.

26. As per claim 23:

The system of claim 22, wherein the digital base band processor is formed as a system on a chip (Official notice is given that a processor can be formed as a system on a chip.).

27. Claim 24 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041), in view of Ramsdale et al. (U.S. 5,265,263), further in view of Dent (U.S. 6,229,796).

28. As per claim 24:

Kotani, Pechanek, and Ramsdale disclosed the system of claim 21, wherein the system is a time-divisional multiple access base station (Ramsdale: Column 2 lines 39-48)

Kotani, Pechanek, and Ramsdale failed to teach wherein the system is a code-division multiple access base station.

However, Dent disclosed wherein the system is a code-division multiple access base station (Dent: Figure 7, column 9 lines 64-67 continued to column 10 lines 1-32).

Both time and code divisional multiple access base station are a ways of allocating frequencies among a plurality of base stations. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that code-divisional multiple access base station could have been substituted for time-divisional multiple access base station.

Response to Arguments

29. The arguments presented by Applicant in the response, received on 1/24/2007 are considered persuasive.

30. Applicant argues that "Kotani and Pechanek failed to teach wherein the direct memory access unit if further to receive and pre-decode a second instruction without sending the pre-decoded second instruction via the output path."

This argument is found to be persuasive for the following reason. The examiner agrees that Kotani and Pechanek didn't disclose this limitation. However, a new ground of rejection has been given that reads upon the limitation.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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